AMENDMENTS TO SPECIFICATION:

Please replace paragraph [0038] with the following amended paragraph:

The lock detection circuit **200**, as shown in Fig. 9 is fundamentally as structure in Fig. 5, except in this embodiment, the output timing signal F_{out} is an input to the frequency divider circuit **225**, and the reference signal F_{ref} is an input to the frequency divider circuit **225**. The ~~input reference signal F_{ref} and the~~ frequency divided ~~signal~~ signals from the frequency divider circuit 225 are applied to a separate phase-frequency detector **205**. The separate phase-frequency detector **205** functions at a different frequency than the phase-frequency detector **10** of Fig. 8. The proportionality of the duration of the deviation output signals **UP 2** and **DOWN 2** of the phase-frequency detector **205** versus the input reference signal F_{ref} is used to determine the amount of deviation or jitter that the phase lock loop can accept before activating the unlock alarm signal **LOCK**. The deviation output signals **UP 2** and **DOWN 2** are logically combined in the OR gate **210** to form the deviation signal **DEV**. The deviation signal **DEV** and the input reference signal F_{ref} are logically combined in the AND gate **215** to form the error signal **ERR**. The error signal **ERR** may be transferred to external circuitry or may be captured and retained in the latch **220** as described above.